Vysoká škola polytechnická Jihlava Katedra elektrotechniky a informatiky

Petri Net Decomposition for FPGA Implementation Seminar annotation

Lecturer: Dr. Ing. Arkadiusz Bukowiec

The presentation shows a new method for the implementation of the application specific logic controllers, constructed using the FPGA devices. The initial steps of the proposed control algorithm rely on the notion of a Petri net, which is an easy way to describe parallel processes. The subsequent steps of the algorithm consist in the decomposition of a given Petri net – with the use of a coloring algorithm – into a set of state machine type subnets. In the results each subnet represents one parallel process. These subnets could be implemented into FPGA device in different ways.

First approach implements all subnets into one FPGA device. The control logic is implemented with use of standard logic cells and the micro-operation generator with use of embedded memory blocks. Second approach implement each subnet independently in different FPGA device to create distributed control system. To ensure proper communication between all subnets, the entire control system uses a globally asynchronous locally synchronous (GALS) architecture. The partial reconfiguration of such controller is also mentioned in the presentation. It allows the dynamic exchange of part of the control algorithm. It could be applied to both approach.